

FIG. 1

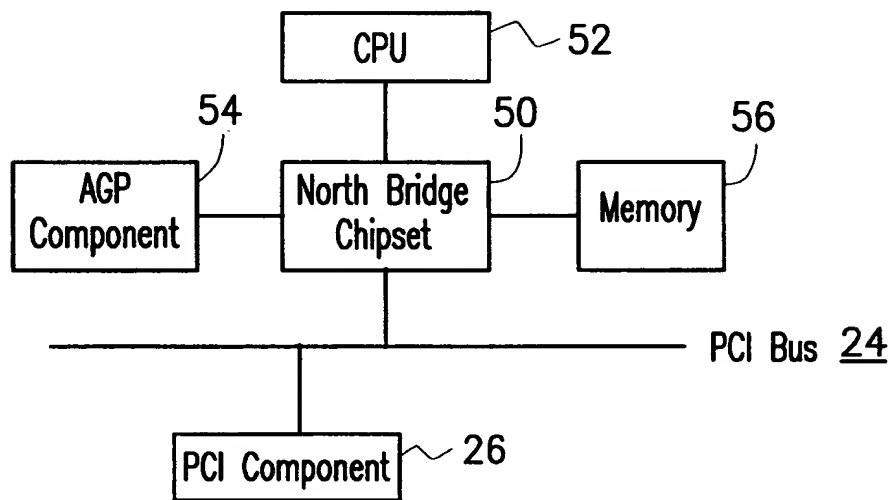


FIG. 2

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graph TD
    START([START]) --> S100[Parameter settings  
1.Total number of simulated operations(fixed value)  
2.FIFO buffer size (fixed value)  
3.Command Sequence/Operation Form(Randomly Generated)  
4.Start Time of Operation(Randomly Generated)]
    S100 --> S104[Component #1]
    S100 --> S134[Component #n]
    S104 --> S108[Idle]
    S108 --> S114[Activate Timer]
    S114 --> S118[Issue one command from the command sequence]
    S118 --> S122{Is command sequence empty?}
    S122 -- YES --> S124[execute the Command]
    S122 -- NO --> S128[Put the Component into idled state]
    S124 --> S160
    S128 --> S160
    S134 --> S138[Idle]
    S138 --> S144[Activate Timer]
    S144 --> S148[Issue one command from the command sequence]
    S148 --> S152{Is command sequence empty?}
    S152 -- YES --> S154[execute the Command]
    S152 -- NO --> S158[Put the Component into idled state]
    S154 --> S160
    S158 --> S160
    S160 --> S162[If two or more of the components are competing for the same resource, such as PCI bus or memory activate the arbiter for arbitration]
    S162 --> END([END])

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FIG. 3